

Features

- 16 x 16 parallel multiplier with double precision product
- 75ns clocked multiply time
- Low power consumption: 120mA
- FS7516 is pin- and function compatible with IDT IDT7216L and Analog Devices AD90109
- Configured for easy array expansion
- User-controlled option for transparent output register mode
- Round control for rounding the MSP
- Input and output directly TTL-compatible
- Three-state output
- Available in a 64-pin DIP

Pin Configuration

X4	1	64	X5
X3	2	63	X6
X2	3	62	X7
X1	4	61	X8
X0	5	60	X9
OELN	6	59	X10
CLKL	7	58	X11
CLKY	8	57	X12
P0, Y0	9	56	X13
P1, Y1	10	55	X14
P2, Y2	11	54	X15
P3, Y3	12	53	CLKX
P4, Y4	13	52	RND
P5, Y5	14	51	XM
P6, Y6	15	50	YM
P7, Y7	16	49	VCC
P8, Y8	17	48	VCC
P9, Y9	18	47	GND
P10, Y10	19	46	GND
P11, Y11	20	45	MSPSELN
P12, Y12	21	44	FT
P13, Y13	22	43	FA
P14, Y14	23	42	OEPN
P15, Y15	24	41	CLKM
P0, P16	25	40	P15, P31
P1, P17	26	39	P14, P30
P2, P18	27	38	P13, P29
P3, P19	28	37	P12, P28
P4, P20	29	36	P11, P27
P5, P21	30	35	P10, P26
P6, P22	31	34	P9, P25
P7, P23	32	33	P8, P24

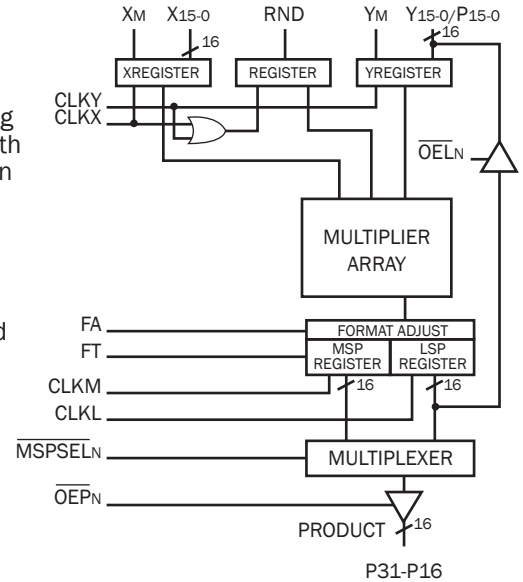
64-PIN DIP TOP VIEW

Description

The Fidus FS7516™ provides an obsolescence solution to the IDT IDT7216L and Analog Devices AD90109 64-pin DIP package. These devices are low power 16 x 16 bit multipliers ideal for fast, real time, digital signal processing (DSP) applications. The FS7516 is designed with readily available devices ensuring confidence in its supply availability.

It is ideal for applications requiring high-speed multiplication such as fast Fourier transform analysis, digital filtering, graphic display systems, speech synthesis and recognition and in meeting any system requirement where multiplication speeds of a microcomputer are inadequate.

All input registers, as well as LSP and MSP output registers, use the same positive edge-triggered D-type flip-flop. In the FS7516, there are independent clocks (CLKX, CLKY, CLKM, CLKL) associated with each of these registers. The FS7516 offers additional flexibility with the FA control and MSPSEL functions. The FA control formats the output for two's complement by shifting the MSP up one bit and then repeating the sign bit in the MSB of the LSP. The MSPSEL low selects the MSP to be available at the product output port, while a high selects the LSP to be available. Keeping this pin low will ensure compatibility with the Analog Devices AD90109.



Functional Block Diagram

Pin Descriptions

Pin name	I/O	Description
X15 - X01	I	X15 - X01 are data inputs
Y15 - Y01	I/O	Y15 - Y01 are data inputs
P15 - P01	O	P15 - P01 are LSP register output, enabled on Pins 9-24 when OELN = 0
P31 - P1	O	Data Output (LSP or MSP dependent upon MSPSELN and OEPN)
OELN	I	Output enable control for LSP (least significant product). When low enables P15 - P01 on pins 9-24. When high P15 - P01 tristated.
OEPN	I	Output enables control for Pins 25-40. When low, output enables Pin 25 - Pin 40. Data output will be dependent upon level of MSPSELN. When this pin is high, Pins 25-40 will be tristated.
XM, YM	I	Mode control for each data word. Low designates unsigned data input and high designates two's complement.
RND	I	"Round" control for rounding of MSP. When high, 1 is added to the most significant bit of LSP. This signal is affected by the state of FA pin. When FA = 1 and RND = 1, 1 is added to the 2-15 bit (P15). When RND = 1 and FA = 0, 1 is added to the 2-16 bit (P14). The RND input is registered. It is clocked on the rising edge of the logical OR of CLKX and CLKY. Rounding always occurs in the positive direction which may introduce a systematic bias.
MSPSELN	I	When low, MSP register output is selected for output on Pins 25-40 and when high, LSP register output is selected for output on Pins 25-40. Output control is done with OEPN.
FA	I	Format adjust control. When high, a full 32 bit product is selected. When low, a left-shifted 31 bit product is selected with the sign bit replicated in the LSP. FA is normally high, except for certain fractional two's complement applications.
FT	I	Flow through control. When high, both MSP and LSP registers are by-passed.
CLKX	I	X register clock input. Also clocks RND register.
CLKY	I	Y register clock input. Also clocks RND register.
CLKL	I	LSP register clock input.
CLKM	I	MSP register clock input.

Absolute Maximum Ratings¹

Symbol	Rating	Industrial	Unit
V _{CC}	Power Supply Voltage	-0.5 to +7	V
V _{term}	Terminal Voltage with Respect to GND	-0.5 to V _{CC} +0.5	V
T _a	Operating Temperature	-40 to +85	°C
T _{stg}	Storage Temperature	-65 to +150	°C
I _{out}	DC Output	50	mA

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Capacitance (T_A = +25°C, f = 1.0 MHz)

Symbol	Parameter ¹	Conditions	Max	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	10	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	12	pF

NOTE:

1. This parameter is measured at characterization and not tested.

DC Electrical Characteristics (Industrial: V_{CC} = 5V ± 10%, T_A = -40°C to +85°C)

Symbol	Parameter	Tests Conditions ¹	Industrial			Unit
			Min.	Typ.	Max	
V _{IH}	Input High Voltage	Guaranteed Logic High Level	2.0	—	—	V
V _{IL}	Input Low Voltage	Guaranteed Logic Low Level	—	—	0.8	V
I _{LI}	Output Leakage Current	V _{CC} = Max., V _{IN} = 0 to V _{CC}	—	—	10	µA
I _{LO}	Output Leakage Current	V _{CC} = Max., OE = 2.0V V _{OUT} = 0 to V _{CC}	—	—	10	µA
I _{CC}	Operating Power Supply Current	V _{CC} = Max., Outputs Disabled f = 10MHz ²	—	40	100	mA
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = -2.0mA	2.4	—	—	V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 8mA	—	—	0.4	V
I _{OS}	Output Short Circuit Current	V _{CC} = Max., V _O = GND	-24	—	—	mA

NOTES:

- 1. Typical implies V_{CC} = 5V and T_A = +25°C.
- 2. I_{CC} is measured at 10MHz and V_{IN} = 0 to 3V.

AC Electrical Characteristics Industrial¹ (V_{CC} = 5V ± 10%, T_A = -40° to +85°C)

Symbol	Parameter	FS7516		Unit
		Min.	Max	
t _{MUC}	Unclocked Multiply Time	—	95	ns
t _{MC}	Clocked Multiply Time	—	75	ns
t _S	X, Y, RND Set-up Time	25	—	ns
t _H	X, Y, RND Hold Time	3	—	ns
t _{PWH}	Clock Pulse Width High	30	—	ns
t _{PWL}	Clock Pulse Width Low	30	—	ns
t _{PDSEL}	MSPSEL _N to Product Out	—	35	ns
t _{PDP}	Output Clock to P	—	35	ns
t _{PDY}	Output Clock to Y	—	35	ns
t _{ENA}	3-State Enable Time	—	25	ns
t _{DIS}	3-State Disable Time	—	25	ns
t _{HCL}	Clock Low Hold Time	0	—	ns

CLKXY Relative to CLKML

NOTE:

1. To ensure that the correct product is entered in the output registers, new data may not be entered into the registers before the output registers have been clocked.

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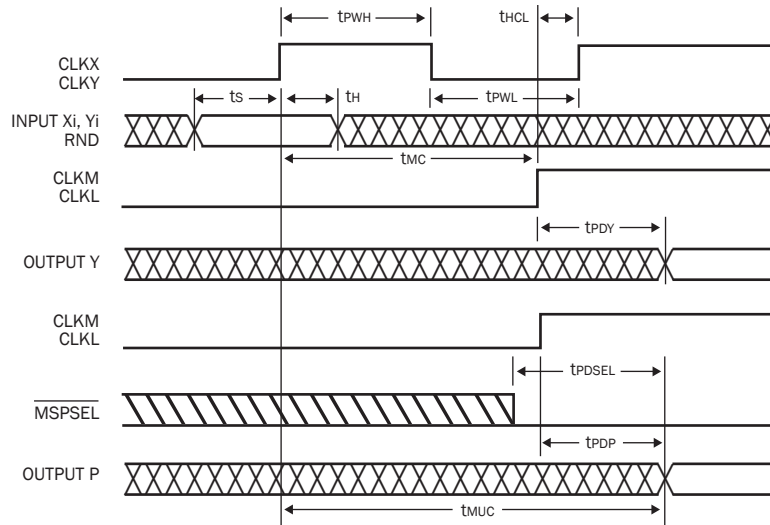
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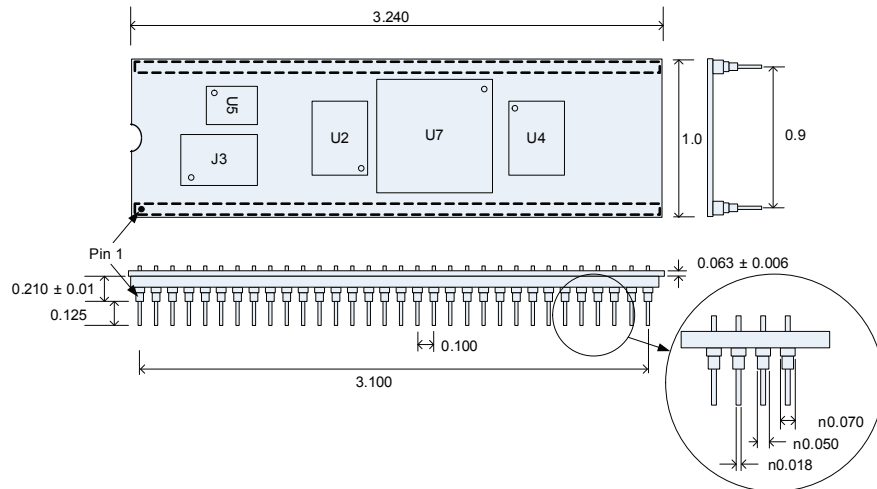
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Timing Diagram



Dimensional Package Outline



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