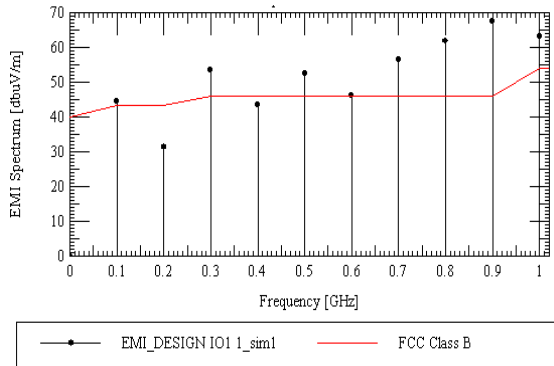


Our capabilities:

Signal/Power Integrity & EMC



Why Choose Fidus?

At Fidus Systems, we understand the unique challenges faced by technology companies – too many projects and too few engineering resources. With top engineering talent, multiple design centers and on-site staffing options, Fidus provides highly responsive engineering teams that are an extension of your development team to successfully bring products to market faster.

Recognized as a trusted design partner, Fidus is dedicated to developing long-term relationships with clients built on integrity, quality and open communications. **With a 97% referral rate, we are proud to say our clients like our work.**

Fidus has delivered more than 800 projects for 215 clients, from Tier-1 multinationals to SMEs to start-ups. Fidus is headquartered in Ottawa, Canada with local design centers in Kitchener-Waterloo and Silicon Valley.

How Can We Help You?

Do you want to: Increase your **revenue**? Reduce your **costs**? Increase your **speed** and **flexibility**? Focus on your **core competency**?

We all do. So consider Fidus for Signal/Power Integrity and EMC Services for your next Product Development, or use our experts in a Consulting facility with all of your on-going programs.

Signal Integrity (SI), Power integrity (PI), and EMC are not big and bad and scary, they are just too often misunderstood or neglected. Time-to-market, repeated Regulatory failures, engineering debug, and PCB re-spin costs are the most apparent results of not carefully considering SI, PI and EMC. The hidden expense of not giving SI, PI, and EMC the proper attention is in the product's Bill of Materials and Assembly costs. These unnecessary product costs are attributed to items such as excessive capacitors, ferrite beads, shields, and manually provisioned RF absorber. The Fidus team helps you avoid these pitfalls.

Our experts average 20 years' experience in this field and are well respected leaders in the Signal Integrity community.

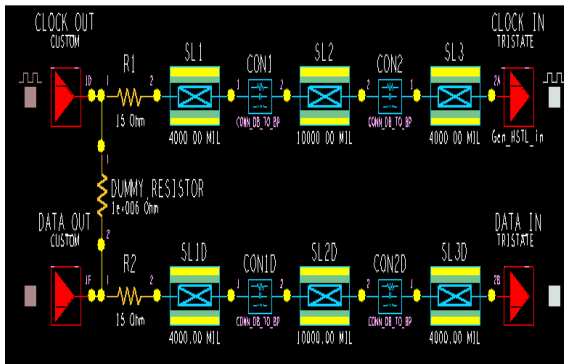
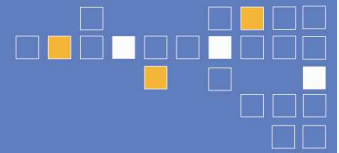
Expertise

Fidus delivers SI, PI, and EMC analysis for on-chip IC design, Package design, PCB-level, and System design.

- Layer stack-up and net topology design
- Pre-layout, during layout, and post-route, high-speed signal integrity analysis and simulation for Verifying signal quality, Reducing signal reflections, Increasing Timing margins, Reducing Crosstalk, Enhancing Power Integrity through cost effective Decoupling design, Simultaneous Switching Noise (SSN) reduction and Reducing conducted and radiated Emissions
- Specific Absorption Rate (SAR) analysis
- Component & system characterization, measured or simulated including full S-parameters, gain & noise figure optimization
- Shield designs for both compliance and sensitive signal preservation

Our Simulation Tools and Equipment

- **Fidus maintains licenses for:** Agilent ADS, ANSYS HFSS, Cadence Allegro PCB SI (SPECCTRAQuest), Cadence PSPICE, Synopsys HSPICE
- **Fidus also has experience with:** Cadence Virtuoso, Cadence Analog Artist and Cadence Spectre, ANSYS Designer, Mentor Graphics HyperLynx
- **RF Laboratory Equipment:** Agilent Network Analyzer, Agilent Vector RF/Signal Generator, Agilent PXA Signal Analyzer, Agilent Digital Signal Analyzer, HP Signal Generators, NHR Power Supply Analyzer, Advantest Spectrum Analyzer, Multi-channel oscilloscopes to 40 GS/s



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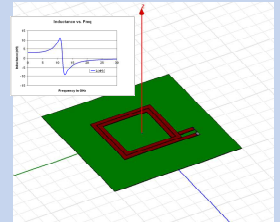
Outside of North America

Contact Michael Wakim at michael.wakim@fidus.com

■ ■ ■ Examples

Integrated Circuit (IC, or on-chip) Design Analysis

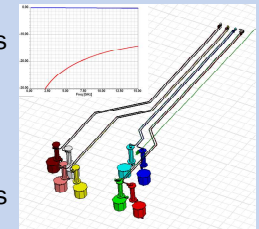
- SSO noise reduction
- IC inductor and transmission-line modeling
- Simulation test bench creation
- DDR2/3 controller characterization and optimization
- Jitter analysis
- Generation of design guidelines, AC characteristics and data sheets



On-Chip Inductor for a wireless Integrated Circuit (IC)

Package Design

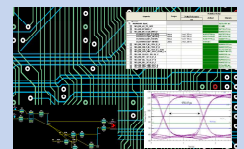
- Package and connector electromagnetic modeling in 3D, leading to equivalent circuits or s - parameters
- Wirebond and flipchip package design with electrical constraints on impedance, cross-talk and delay
- Optimization of interconnects for frequencies up to 12GHz



Gbps differential package layout

Printed Circuit Board (PCB) Analysis

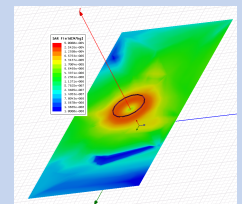
- Printed Circuit Board (PCB) modeling and constraint management
- Creation of topology templates and routing guidelines
- Pre- and Post-route simulation



Printed Circuit Board Signal Integrity (PCBSI)

System Design

- Power, grounding, decoupling and filtering analysis
- Multi-board system simulations
- High-speed backplanes
- Multi-Gigabit serial links
- 3D Enclosure modeling for EMI
- Specific Absorption Rate (SAR) computation



Low frequency SAR in the skin layer due to a loop antenna